

FORM PTO-1449 <i>O I P E</i> APR 01 2004 U.S. PATENT & TRADEMARK OFFICE	U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE INFORMATION DISCLOSURE STATEMENT BY APPLICANTS	ATTY. DOCKET NO. ALT-323 Cont. Div.	APPLICATION NO. 10/702,300
		APPLICANTS Bonnie I. Wang et al.	CONFIRMATION NO. 7980
		FILING DATE November 5, 2003	GROUP ART UNIT

U.S. PATENT DOCUMENTS

EXAMINER INITIAL	DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE IF APPROPRIATE
	5,059,924	10/22/91	JenningsCheck	331	25	
	5,170,297	12/08/92	Wahler et al.	360	51	
	5,185,581	02/09/93	Brown	331	108B	
	5,298,866	03/29/94	Kaplinsky	328	155	
	5,451,912	09/19/95	Torode	331	1A	
	5,561,692	10/01/96	Maitland et al.	327	153	
	5,635,879	06/03/97	Sutardja et al.	331	135	
	5,642,082	06/24/97	Jefferson	331	25	
	5,699,020	12/16/97	Jefferson	331	17	
	5,701,270	12/23/97	Rao	365	230.03	
	5,731,743	03/24/98	Sauer	331	57	
	5,744,991	04/28/98	Jefferson et al.	327	158	
	5,889,436	03/30/99	Yeung et al.	331	25	
	5,896,346	04/20/99	Dell et al.	365	233	
	5,963,069	10/05/99	Jefferson et al.	327	158	
	5,970,110	10/19/99	Li	327	147	
	6,100,735	08/08/00	Lu	327	158	
	6,114,915	09/05/00	Huang et al.	331	25	
	6,326,812	12/04/01	Jefferson	326	93	
	6,329,850	12/11/01	Mair et al.	327	156	

FOREIGN PATENT DOCUMENTS

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OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)

EXAMINER INITIAL	
KL	Wolaver, Dan H., <i>Phase-Locked Loop Circuit Design</i> , PTR Prentice Hall, Englewood Cliffs, New Jersey, 1991, pp. 68-70
KL	"ORCA® OR3Cxx (5 V) and OR3Txxx (3.3 V) Series Field-Programmable Gate Arrays," Lucent Technologies Microelectronics Group, Preliminary Data Sheet, November 1997

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